MADCAP Layered Packaging

MADCAP Program

Mosaic Array Data Compression and Processing

USASSDC CONTRACT DASG60-90-C-0136

BOEING®

ON-FPA Signal Processing

- The overall objective is to increase signal to noise and the signal dynamic range — digitizing the data prior to transmission off the focal plane is a typical application
- Special situations impose more specific requirements
  - Seeing in a radiation environment imposes high sampling rates and a requirement for non-linear filters on the focal plane
  - Analog filtering to remove background is most effectively done on the focal plane
  - Spatial filtering to increase the usable dynamic range is most effectively done on the focal plane

MADCAP History and Near Term Objectives

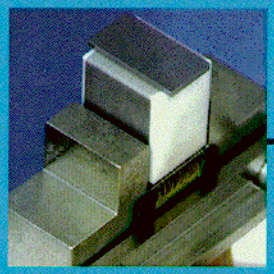
FY91 Go-Ahead

FY94

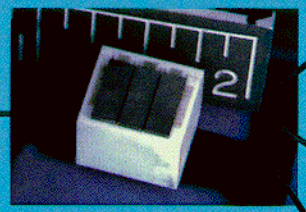
FY96

FY97

- **FPA substrate module**
  - Low cost
  - Low thermal mass for strategic and tactical

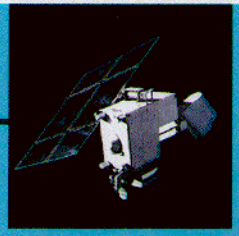


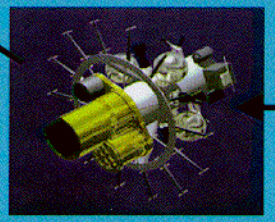
Early Module



3-Color Module

Digital Interface Modular Design Supports Both Strategic and Tactical Products

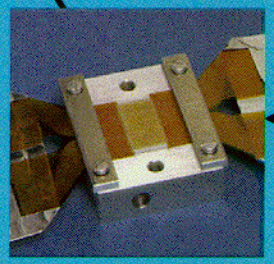




Gamma Filter for Far Term Hardening

3-color module highly integrated design

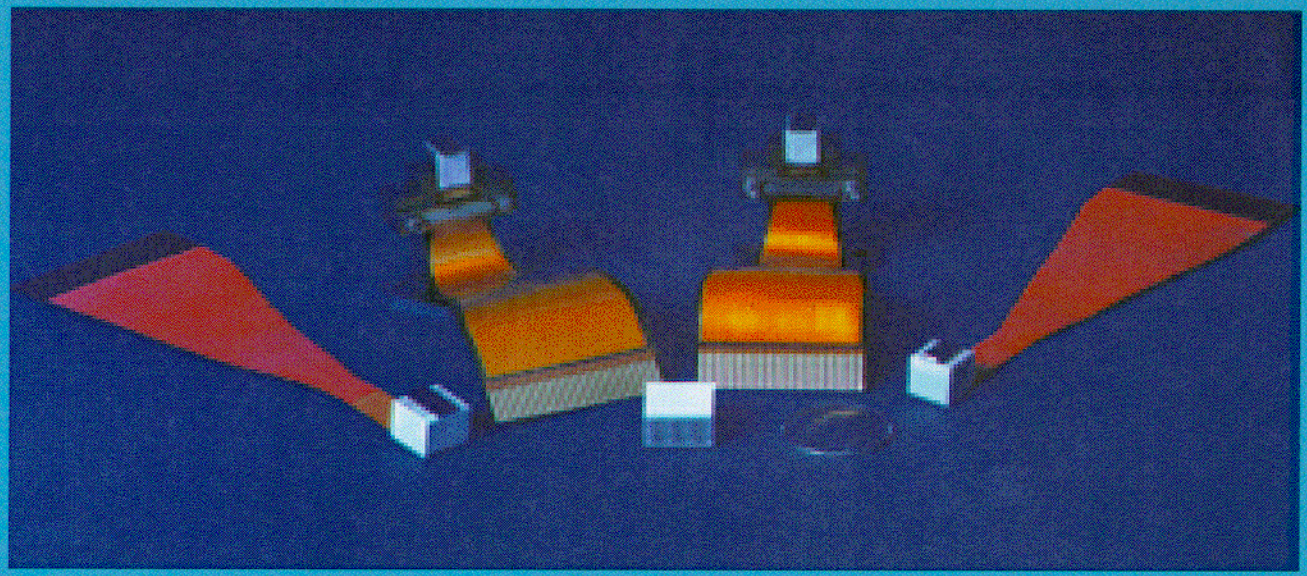
- Preamplification
- 12 bit analog to digital conversion
- Dynamic range compression
- Responsivity correction
- Gamma pulse circumvention
- Time delay integration
- Multiplexing
- Onboard controls and memory



Special Applications

BOEING

MADCAP Focal Plane Modules

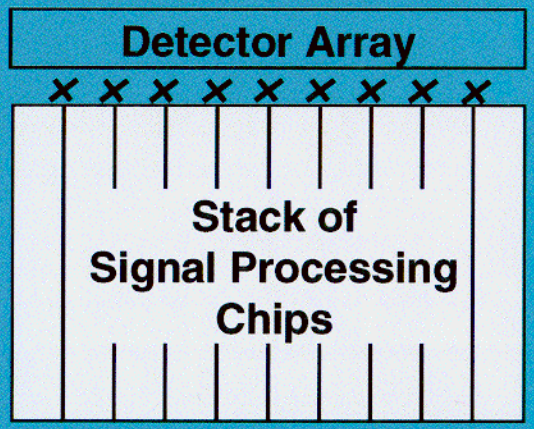


- Three generations of MADCAP modules have been fabricated and tested
  - Each generation introduced a packaging improvement leading to the high yield flip-chip platelet
  - Signal processing functions evolved to include all of the contract goals including a gamma circumvention, TDI, gain/offset correction, filtering and 12 bit analog to digital conversion

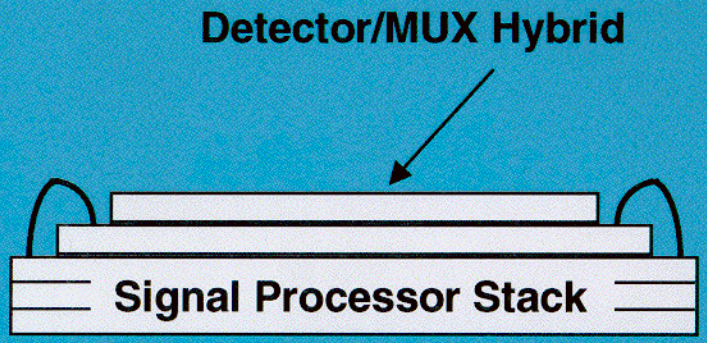
Package Design

- There are two development parts to the Focal Plane Module
  - Design of the low power custom logic
  - Design and processing definition for cryo multilayer package
- The package and custom logic support each other
  - Because it is simple the package can be made thin enough to support several die in a low mass module
  - The IC design supports the simple package structure, (single interconnect layer per die), by multiplexing data according to a die location address
- MADCAP module assembly contains several square inches of silicon

Module Configurations

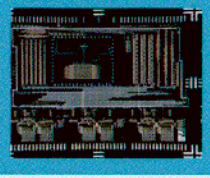


- The vertical stack mates on-edge to the detector array
  - Hard wire contact between each detector and the supporting electronics
  - Requires precision assembly



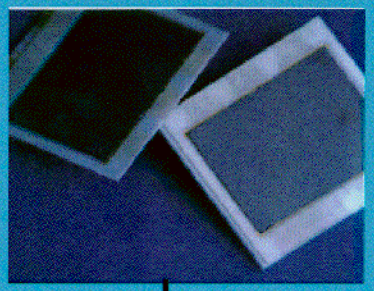
- The horizontal stack is wire bonded to a detector readout chip
  - Low cost and relaxed tolerances
  - Several square inches of silicon area

Interconnecting Flip-Chip Hybrid Package

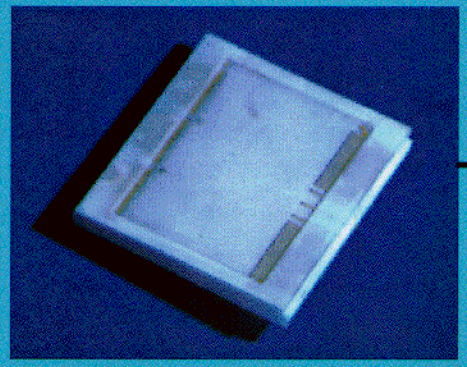


Signal Processing Chips

- Designed to operate at FPA temperatures with milliwatt power
- Chips are thinned

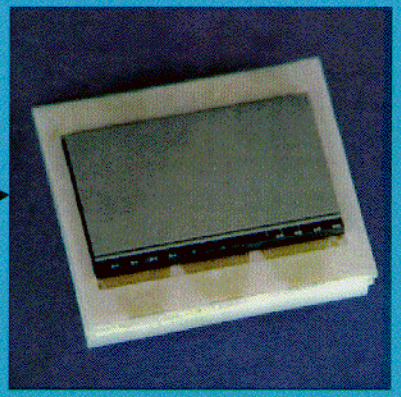


Chips are mounted to thin interconnecting ceramic carriers that can be stacked to form a signal processing module



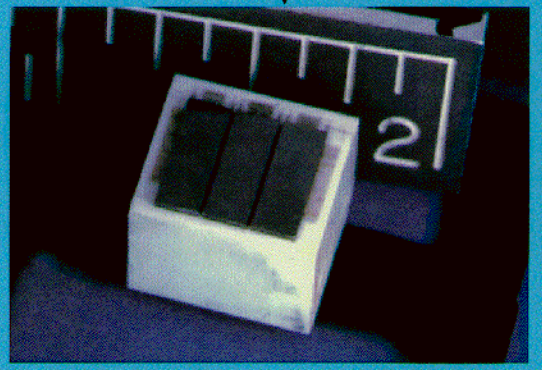
The Interconnected Module

With wire bond pads for mounting the detector array hybrid



Mounted 256 x 256 Hybrid

Module is a 5 layer design that would support large area focal plane arrays



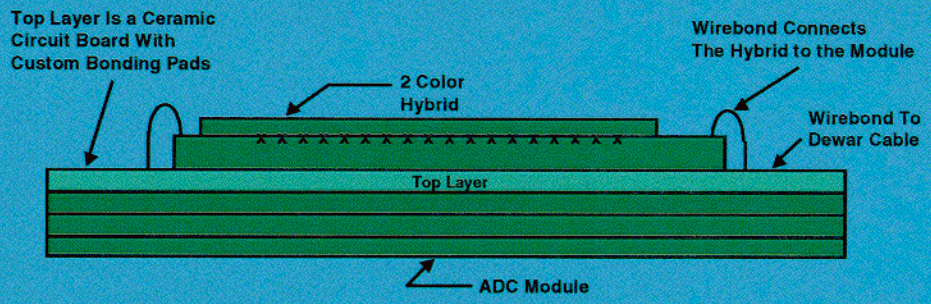
Technology Demonstration Module

- 3 colors (1728 detectors)
- Total power 50 mw
- Gamma filter, TDI gain/offset and analog to digital conversion

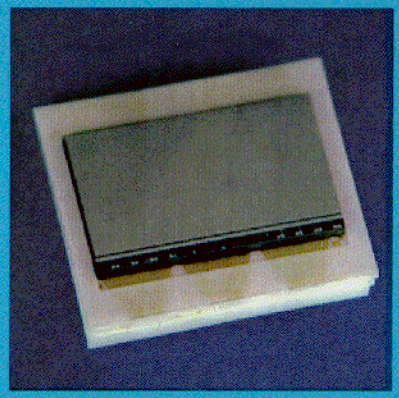
BOEING®

"Bolt-On" Module

- The current MADCAP contract has funding to deliver a module in early 1998



CE Configuration with two ADC chips

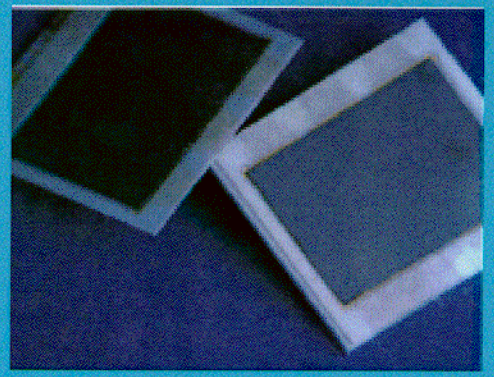


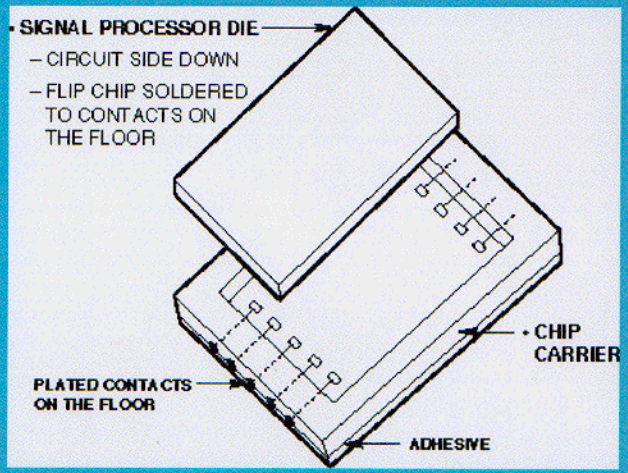
Mounted 256 x 256 Hybrid (Mockup Module)

- The module will contain two 10 Msps ADC chips to support a two color 256 x 256 detector hybrid – the DITP 512 x 512 two color array requires 4 chips
- The chip carrier configuration will accommodate different hybrids with modification of the top layer interconnect

Module Layer Structure

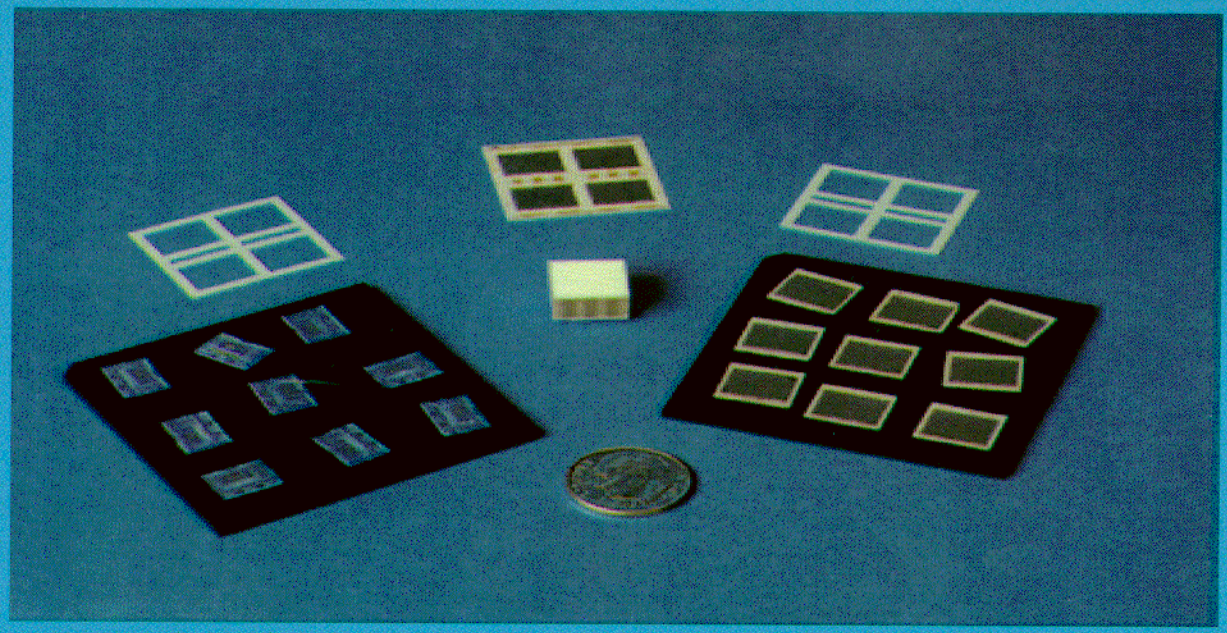
- The flip-chip carrier supports stacking die and accommodates existing semiconductor devices/processes
- Ceramic is strong, stable and has good thermal conductivity
- Ceramic substrate isolates the conductive die substrate and supports interconnect lines
- Ceramic window supports the stack, provides a bonding surface, and the surface for interconnecting the module





BOEING®

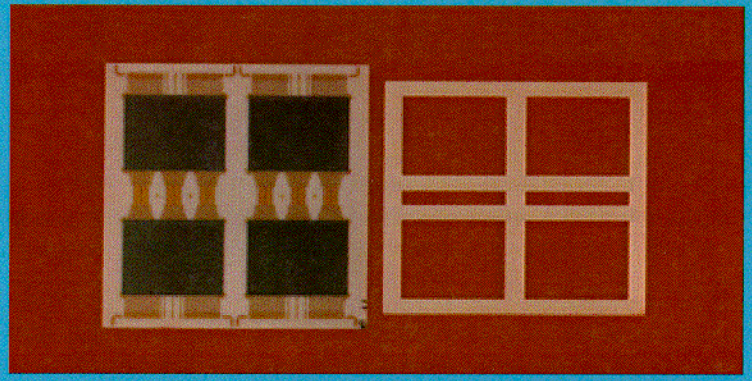
Flip-Chip Platelet Assembly



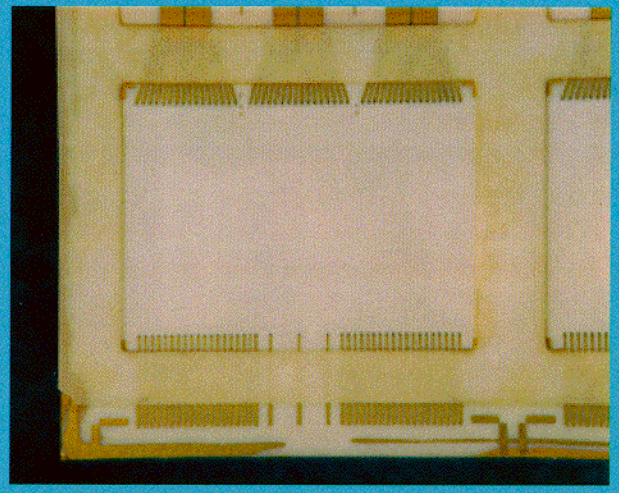
- Several hundred 4 mil platelets were fabricated to assemble the technology demonstration modules
  - Assembly yield over 50%
  - Critical module assembly steps
    - Die thinning
    - Contact deposition
    - Flip-chip mating
    - Platelet thinning
    - Stacking
    - Metalization

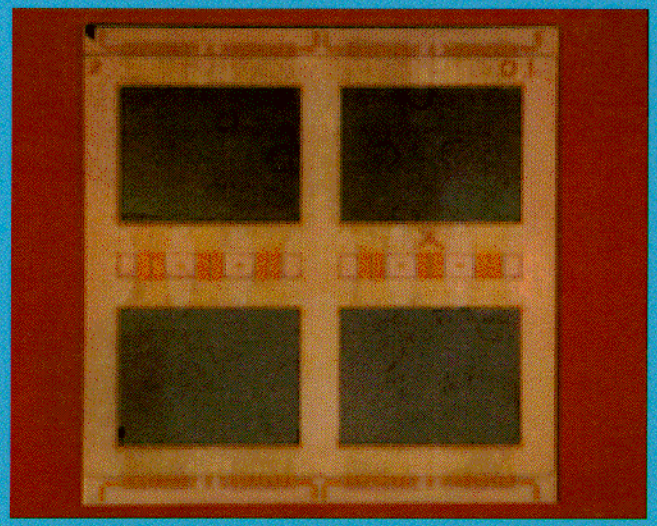
Platelet Assembly

- **Platelets 4.5 mils thick have been fabricated**
  1) Thinned die are flip-chip mounted to floors
  2) Windows are added
  3) Platelets are diced out of the arrays



An array of four flip-chip mounted die with unmounted windows

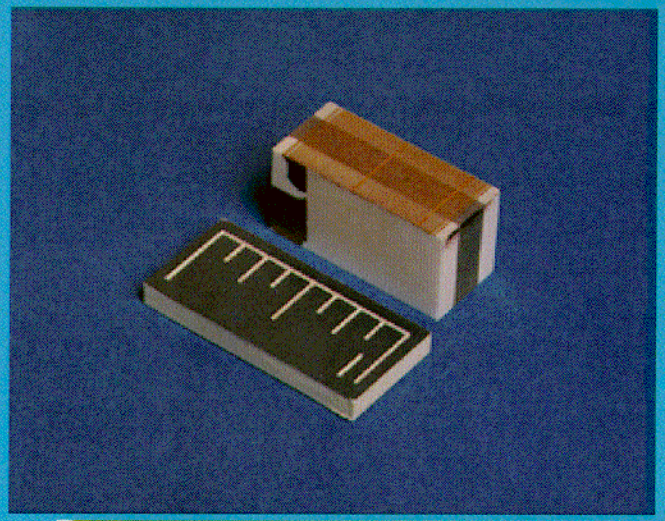


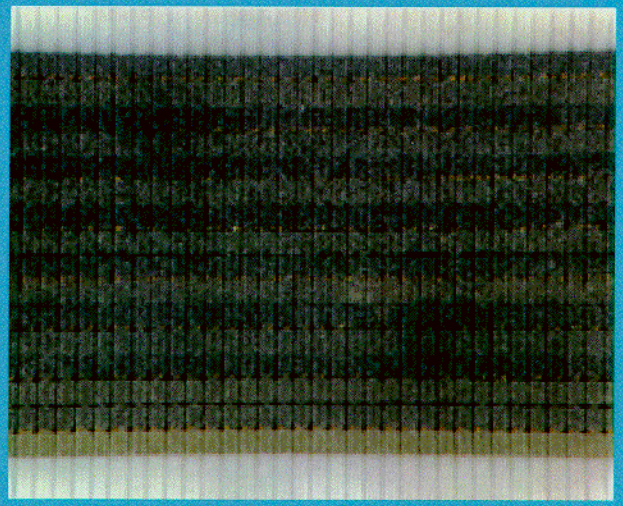


An array of 4 platelets

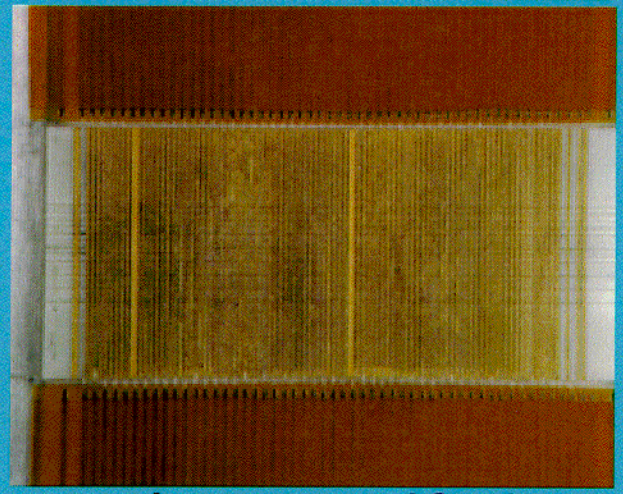
Module Interconnect

- Groove and polish module interconnect
  - Interconnect stacks with large numbers of platelets
  - Visual alignment
  - Thick gold conductor





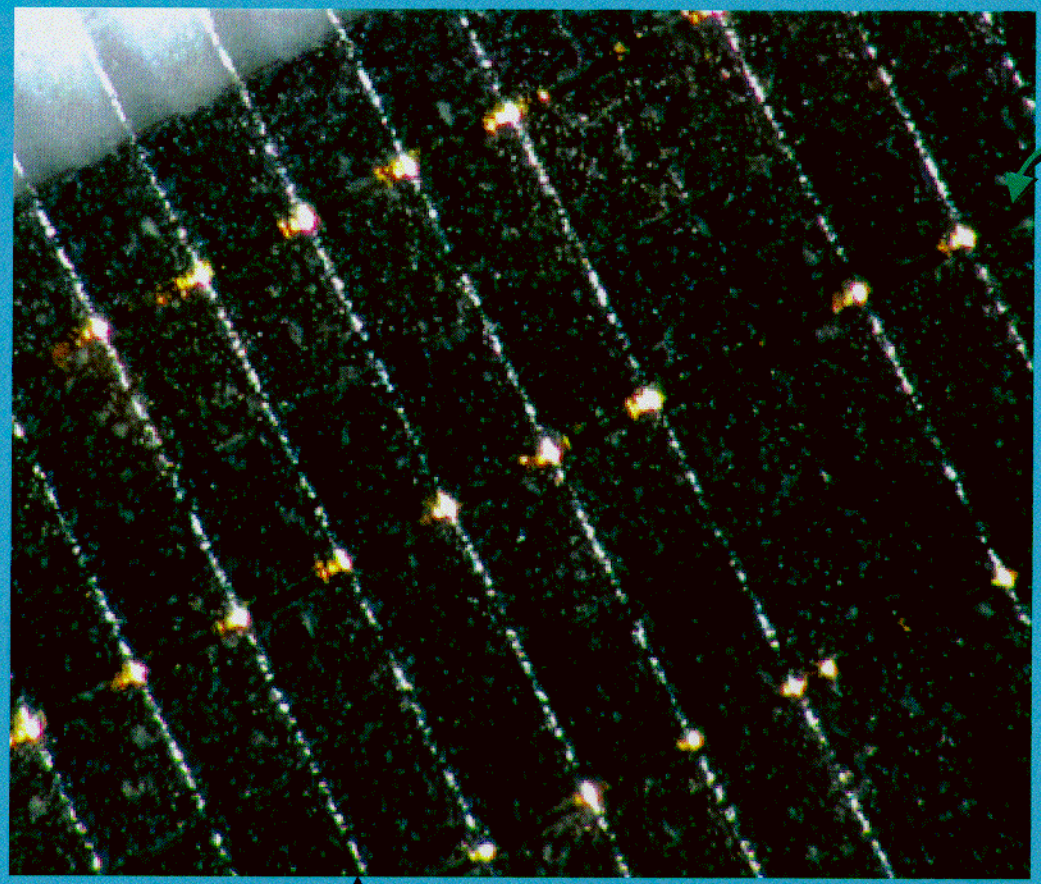
Contact Grooves



Interconnected Stack

BOEING®

Interconnect Alignment

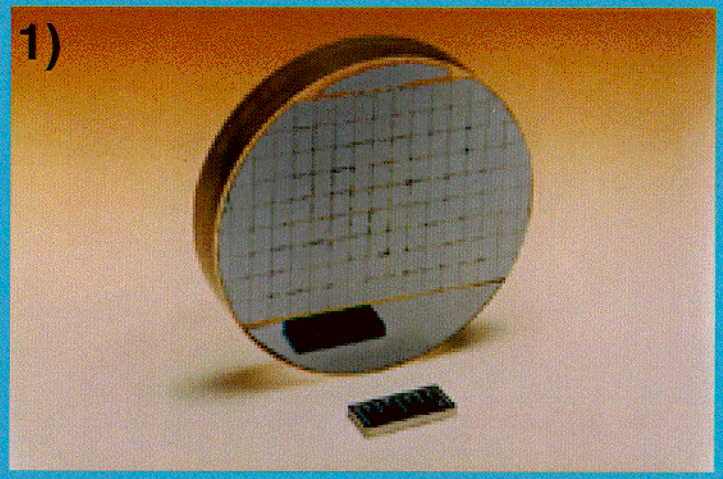


Exposed Contacts

Grooves on the surface of the module cut through the contacts from each platelet — mechanical alignment (visual)

BOEING®

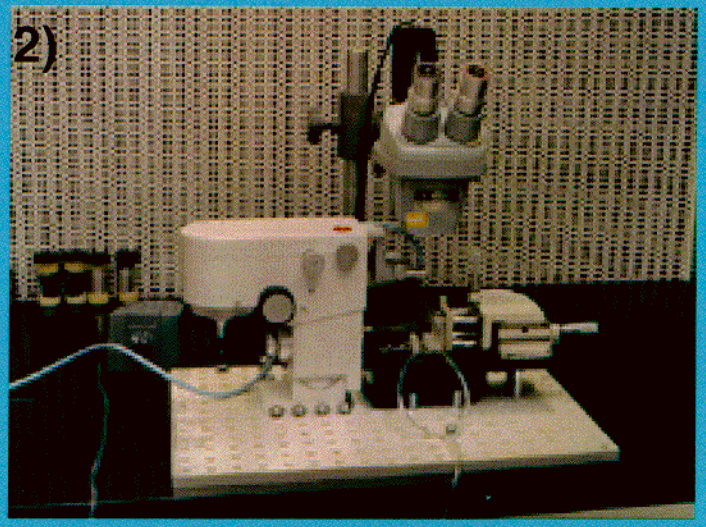
Critical Process Steps

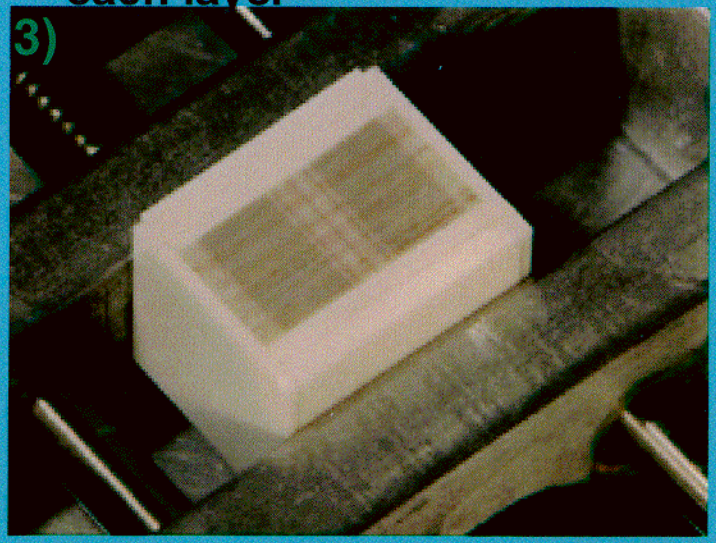


1) A grooved wafer mounted to a polishing block is thinned to yield 3 mil thick die

2) Stacking modules is a mechanical process - alignment ± 15 microns

3) Module interconnect requires robust conductors that contact each layer





BOEING

Important Design Constraints

- The modules are mechanically assembled so that tolerances are larger than photolithographic processes
- Thick interconnect contacts improve operability
- Thick interconnect lines avoid opens due to step coverage

Conclusion

- There are two interdependent technologies required to develop a successful focal plane module
  - Low power custom integrated circuit designs that operate within the sensor constraints
  - The most basic package that will allow shielding, electrical isolation and interconnection of a number of integrated circuits
- The majority of this work has focused on custom applications